ABSTRACT

An integrated circuit having devices fabricated in both SOI regions and bulk regions, wherein the regions are connected by a trench filled with epitaxially deposited material. The filled trench provides a continuous semiconductor surface joining the SOI and bulk regions. The SOI and bulk regions may have the same or different crystal orientations. The present integrated circuit is made by forming a substrate with SOI and bulk regions separated by an embedded sidewall spacer (made of dielectric). The sidewall spacer is etched, forming a trench that is subsequently filled with epitaxial material. After planarizing, the substrate has SOI and bulk regions with a continuous semiconductor surface. A butted P-N junction and silicide layer can provide electrical connection between the SOI and bulk regions.